What is claimed is:

1. A device for recovering a burst-mode clock, the device comprising:

signal forming means including a first delay unit and an exclusive OR gate having two inputs and one output, wherein a random signal sequence is applied to an input of the first delay unit and one input of the exclusive OR gate and an output of the first delay unit is applied to the other input of the exclusive Or gate;

reference clock generating means including a second delay unit and a first logic element, wherein a logic operation is implemented with respect to a signal output from the signal forming means and a signal output from the signal forming means and delayed by the second delay unit to generate a reference clock;

feedback means including a third delay unit for delaying a final output signal, an OR gate for implementing an OR operation with respect to a signal output from the signal forming means and a signal delayed in the third delay unit and a fourth delay unit for delaying an output of the OR gate to synchronize with the reference clock; and

correcting means for correcting a duty of the final output signal according to an output of the reference clock generating means by implementing a logic operation with respect to outputs of the feedback means and the reference clock generating means.

2. The device of claim 1, wherein when a period of the random signal sequence is T, the first delay unit, the second delay unit and the fourth delay unit are delayed by as long as T/2 and the third delay unit is delayed by as long as T.

3. The device of claim 1, wherein in the reference clock generating means, a NOR operation is implemented with respect to the signal output from the signal forming means and the signal output from the signal forming means and delayed by the second delay unit, and the correcting means includes an AND gate.